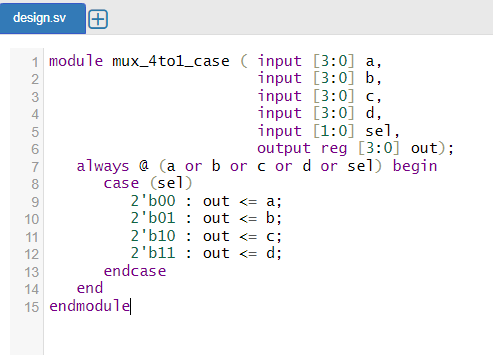
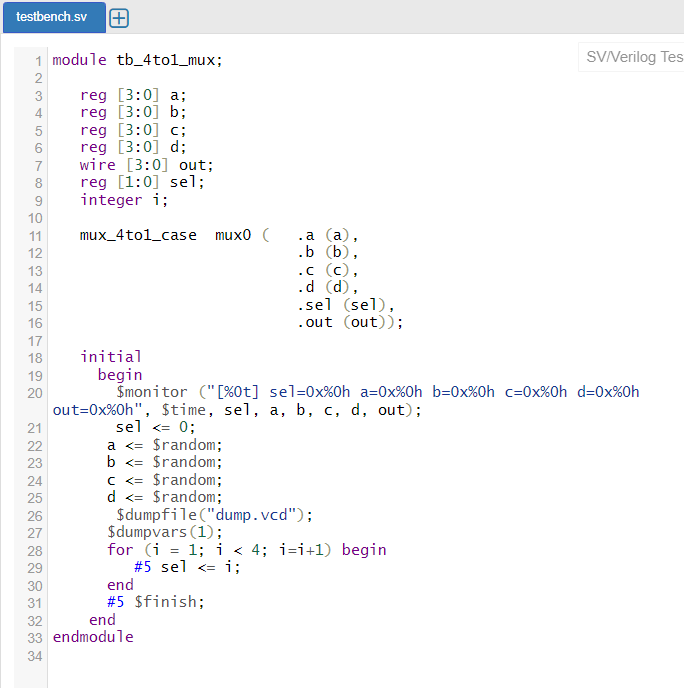
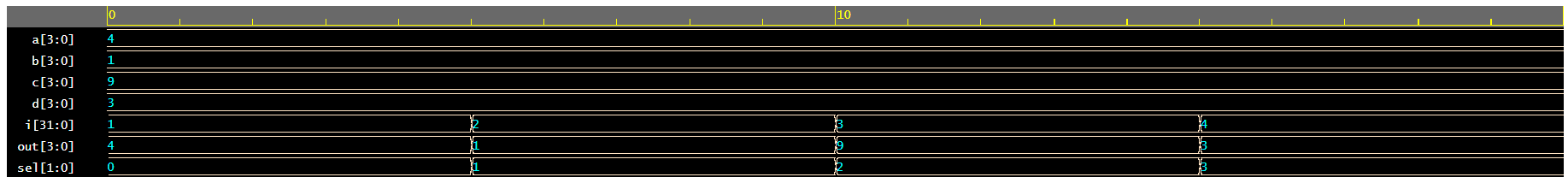
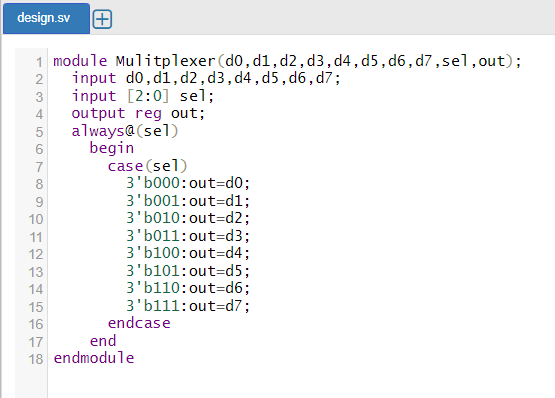
**LAB 6: Designing of Multiplexer, Demultiplexer, Decoder, Encoder**

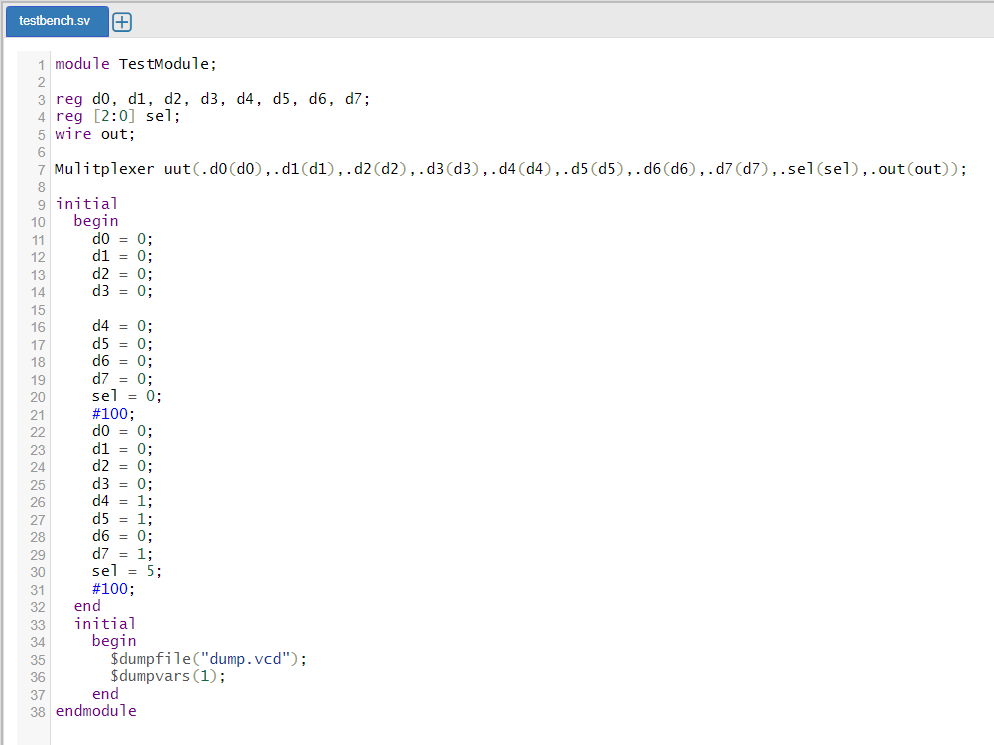
**Question 1: Write a Verilog code to design a 4:1 Multiplexer and verify the same.**

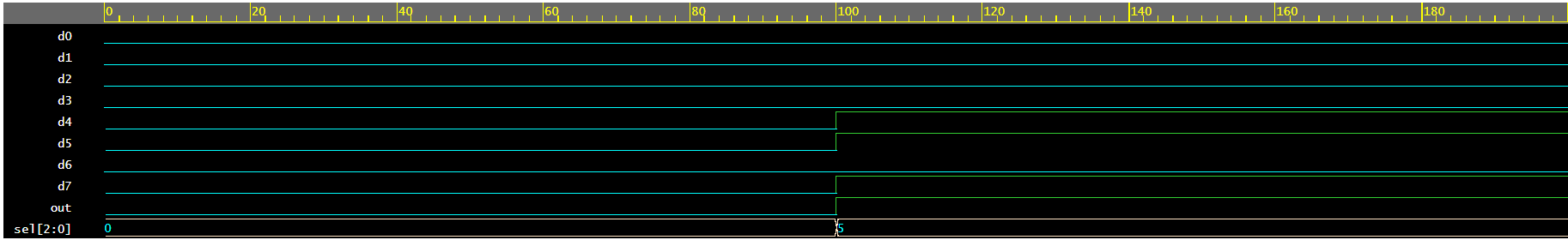
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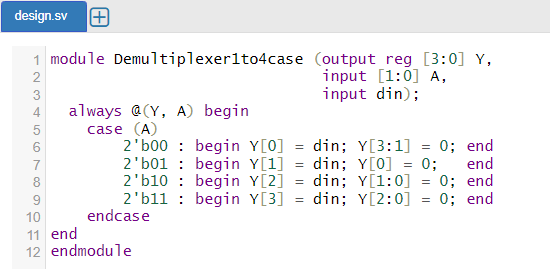
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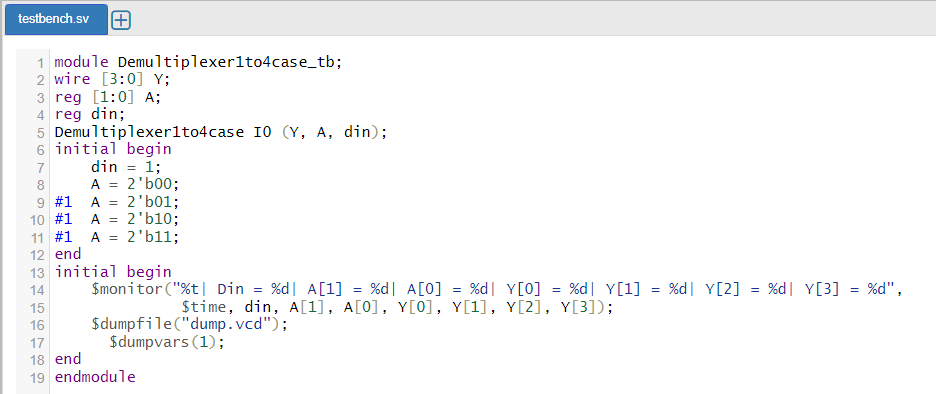
**Question 2: Write a Verilog code to design an 8:1 Multiplexer and verify the same.**

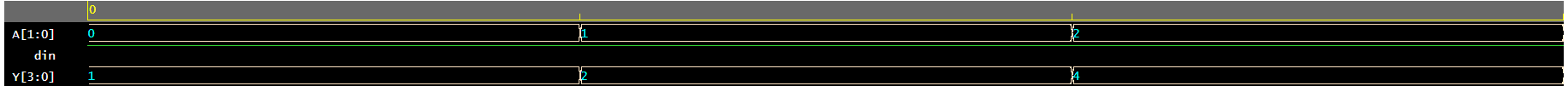
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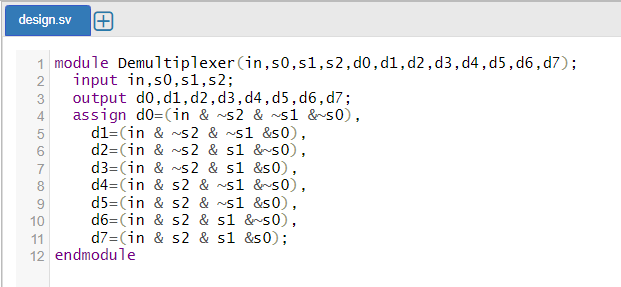
**Question 3: Write a Verilog code to design a 1:4 Demultiplexer and verify the same.**

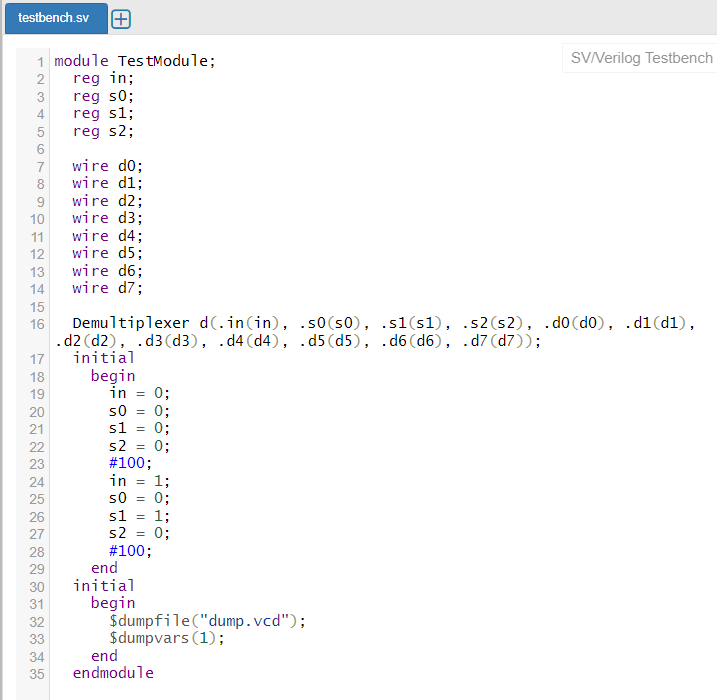
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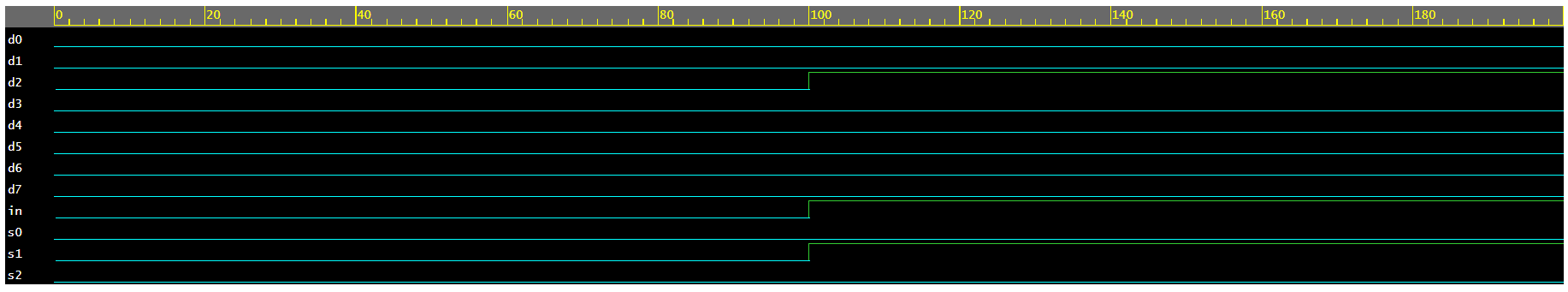
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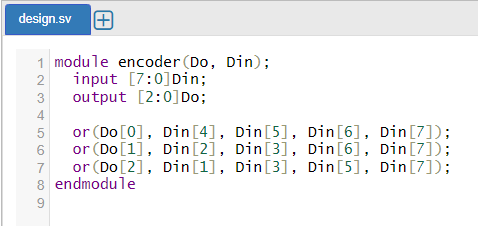
**Question 4: Write a Verilog code to design a 1:8 Demultiplexer and verify the same.**

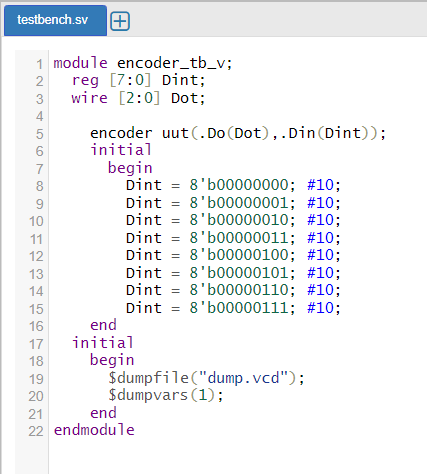
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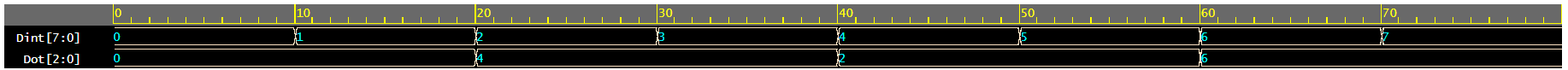
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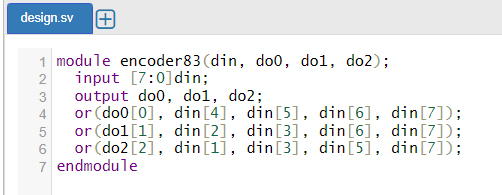
**Question 5: Write a Verilog code to design a 3:8 Decoder and verify the same.**

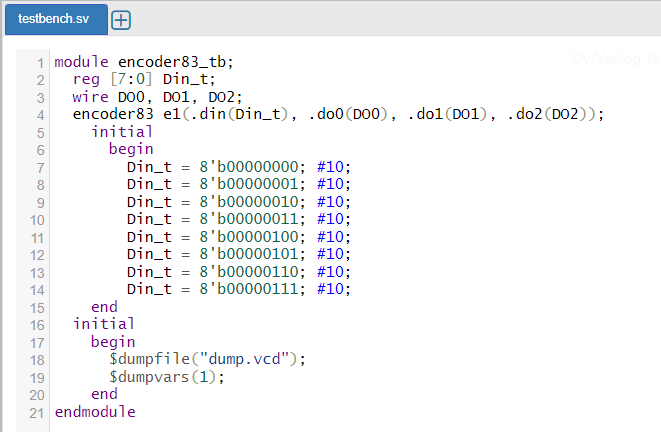
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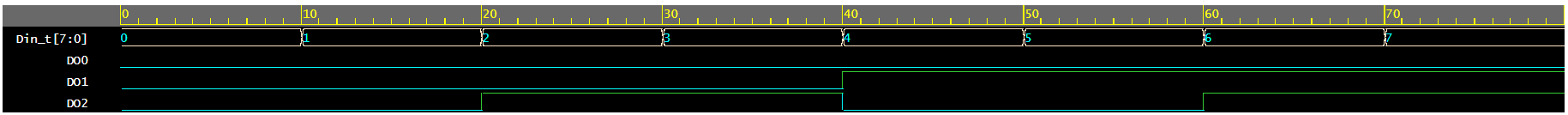
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**Question 6: Write a Verilog code to design a 8:3 Encoder and verify the same.**

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